IN THE CLAIMS

PLEASE ADD THE FOLLOWING NEW CLAIMS

14. A Dual Damascene wiring structure, integrating low-K dielectrics, for use in semiconductor fabrication, comprising:

a semiconductor structure having a surface containing conductive regions and insulating regions;

a dielectric layer overlaying the substrate and in contact with the conductive regions and the insulating regions; the dielectric layer having a planar top surface, the dielectric layer comprised of a single homogeneous low-K material, the low-K material having a dielectric constant of less than about 3.2;

a matrix of structural openings in the dielectric layer extending to the insulating regions; the structural openings containing a thermally conductive structural material in contact with the insulating regions and planar with the top surface of the dielectric layer, whereby a matrix of structural elements is embedded within the dielectric layer.

a plurality of via openings in the dielectric layer extending to the conductive regions, the via openings containing a conductive material in contact with the conductive regions and planar with the top surface of the dielectric layer; wherein a plurality of conductive vias provides electrical communication through the dielectric layer;

a plurality of interconnect openings in the top surface of the dielectric layer and extending partially through the dielectric layer, said interconnect openings extending along the surface of the dielectric layer and contacting at least one via opening, the interconnect openings containing the conductive material in contact with the conductive material in the via opening and planar with the top surface of the dielectric layer; wherein a plurality of conductive interconnects cooperating with the plurality of conductive vias provide electrical communication throughout the dielectric layer;

whereby a thermally and electrically communicative low-K dielectric structural layer is provided for semiconductor fabrication.

15. The Dual Damascene wiring structure of Claim 14, wherein the low-K dielectric material comprises a material selected from the group composed of: aerogel, xerogel, nanogel, Flare, amphoric Cfx, JSR, Coral and Black Diamond.

16. The Dual Damascene wiring structure of Claim 14, wherein the thermally conductive structural material comprises a material selected from the group composed of: silicon nitride, silicon carbide, amorphous carbon, carbon, tungsten, copper and aluminum.

17. The Dual Damascene wiring structure of Claim 14, wherein the conductive material comprises a material selected from the group composed of: tungsten, copper

and aluminum.

18. The Dual Damascene wiring structure of Claim 14, wherein a conformal barrier layer lining the via openings and the interconnect openings separates the low-K dielectric from the materials within the openings, said barrier layer comprising tantalum nitride.

19. The Dual Damascene wiring structure of Claim 14, wherein the top surface of the dielectric providing insulating region and having planar conductive interconnects and vias forming conductive regions, the wiring structure is capable of replication.

20. A Single Damascene wiring structure, integrating low-K dielectrics, for use in semiconductor fabrication, comprising:

a semiconductor structure having a surface containing conductive regions and insulating regions, the conductive regions further comprising a first plurality of conductive interconnects atop the surface;

a dielectric layer overlaying the substrate and in contact with the conductive regions and the insulating regions; the dielectric layer having a planar top surface, the dielectric layer comprised of a single homogeneous low-K material, the low-K material having a dielectric constant of less than about 3.2;

a matrix of structural openings in the dielectric layer extending to the insulating regions; the structural openings containing a thermally conductive structural material in contact with the insulating regions and planar with the top surface of the dielectric layer, whereby a matrix of structural elements is embedded within the dielectric layer.

a plurality of via openings in the dielectric layer extending to the conductive regions, the via openings containing a conductive material in contact with the conductive regions and planar with the top surface of the dielectric layer; wherein a plurality of conductive vias provides electrical communication through the dielectric layer;

a second plurality of interconnects formed from the conductive material overlaying the top surface of the dielectric layer, extending along the surface of the dielectric layer and contacting at least one conductive via, wherein the plurality of conductive interconnects cooperating with the plurality of conductive vias provide electrical communication throughout the dielectric layer;

whereby a thermally and electrically communicative low-K dielectric structural layer is provided for semiconductor fabrication.

21. The Single Damascene wiring structure of Claim 20, wherein the low-K dielectric material comprises a material selected from the group composed of: aerogel, xerogel, nanogel, Flare, amphoric Cfx, JSR, Coral and Black Diamond.

22. The Single Damascene wiring structure of Claim 20, wherein the thermally conductive structural material comprises a material selected from the group composed of: silicon nitride, silicon carbide, amorphous carbon, carbon, tungsten, copper and aluminum.

23. The Single Damascene wiring structure of Claim 20, wherein a conformal barrier layer lining the via openings and the interconnect openings separates the low-K dielectric and the materials within the openings, said barrier layer comprising tantalum nitride.

24. The Single Damascene wiring structure of Claim 20, wherein a conformal barrier layer lining the via openings separates the low-K dielectric from the materials within the openings, said barrier layer comprising tantalum nitride.

25. The Single Damascene wiring structure of Claim 20, wherein the top surface of the dielectric providing insulating regions and having conductive interconnects and planar vias forming conductive regions, the wiring structure is capable of replication.